1 0

1.4 2024.4

0.1	2018.12	Initial revision
0.2	2019.8	Add DC characteristics and footprint
0.3	2019.9	Add ordering information
0.4	2019.10	Change Emerald to WX1860, update section 1.3.4
0.5	2019.11	Update pin description
0.6	2019.11	Add suggested SPI flash and MDI signal description
0.7	2019.12	Add IO DC specification
0.8	2020.7	Add single-port WX1860A1 and WX1860AL1
0.9	2020.12	Update clock input description
1.0	2021.1	Update duplex mode support
1.1	2021.11	Update order information
1.2	2023.6	Add SPI clock description
1.3	2023.9	Updated chip working current
1.4	2024.4	Add description of power on timing Delete Competitive product description

1

1.1

10/100/1000 Copper PHY integrated on-chip	1/2/4 ports
Jumbo frames supported	9.5 KB
Flow control support: send/receive PAUSE frames and receive FIFO thresholds	Y
Statistics for management and RMON	Y
802.1q VLAN support	Y
802.3az EEE support	Y
MDI Flip	Y
SerDes interface for external PHY connection or system interconnect	N
1000BASE-KX interface for Blade Server Backplane connections	N
802.3ap Backplane Auto-negotiation	N
SGMII interface for external 1000BASE-T PHY connection	N
RGMII interface for external PHY	1/2/4 ports
Fiber/copper auto-sense	N
SerDes support of non-Auto-Negotiation partner	N
SerDes signal detect	N
External PHY control I/F MDC/MDIO	perfunction
External PHY control I/F 2 wire I/F	perfunction

IPsec with SM4-GCM algorithm	Y
LinkSec with SM4-GCM algorithm	Y
Duplex mode support	Full duplex

1.2

Max Link Speed	Gen2x4
Max Payload Size	128 B
Max Read Request Size	128 B
VPD	Y
ECRC	Y
LTR	N
CSR access via Configuration space	N
ACS	N
AER	Y
Multiple PF	4
DCA support	N
TPH support	Y
PF FLR	Y
SR-IOV	8VF/PF
VF AER	Y

VF FLR	Y
64-bit BAR	Y
MSI	Y
MSI-X	32/PF
VF MSI-X	2/VF

1.3

Programmable host memory receive buffers	Y
Descriptor ring management hardware for transmit and receive	Y
Software controlled global reset bit (resets everything except the configuration registers)	Y
Software Definable Pins (SDP) - per port	4
Four SDP pins can be configured as general purpose interrupts	Y
Wake up	Y
Flexible wake-up filters	8
Flexible filters for queue assignment in normal operation	N
IPv6 wake-up filters	Y
Default configuration by the EEPROM for all LEDs for pre-driver functionality	4 LED
LAN function disable capability	Y
Programmable memory transmit buffers	Y

Double VLAN	Y
IEEE 1588	Y
Per-Packet Timestamp	N
TX rate limiting per queue	N
TCP segmentation offload Up to 256 KB	Y
iSCSI TCP segmentation offload (CRC)	N
IPv6 support for IP/TCP and IP/UDP receive checksum offload	Y
Fragmented UDP checksum offload for packet reassembly	Y
Message Signaled Interrupts (MSI)	Y
Message Signaled Interrupts (MSI-X) number of vectors	36
Packet interrupt coalescing timers (packet timers) and absolute delay interrupt timers for both transmit and receive operation	Y
Interrupt throttling control to limit maximum interrupt rate and improve CPU utilization	Y
Rx packet split header	Y
Receive Side Scaling (RSS) number of queues per port	up to 8
Total number of Rx queues per port	8
Total number of TX queues per port	8
RX header replication	N
Low latency interrupt	Y
TCP timer interrupts	Y
No snoop	Y

Relax ordering	Y
TSO interleaving for reduced latency	Y

1.4

Support for Virtual Machines Device queues (VMDq) per port	8 pools single queue
L2 MAC address filters (unicast and multicast)	32
L2 VLAN filters	per pool
PCI-SIG SR-IOV	8 VF
Multicast/Broadcast Packet replication	Y
VM to VM Packet forwarding (Packet Loopback)	Y
MAC and VLAN anti-spoofing	Y
Per-pool statistics	Y
Per-pool off loads	Y
Per-pool jumbo support	Y
Mirroring rules	4
External switch VEPA support	Y
Promiscuous modes	VLAN, unicast, multicast
ETAG	Y

1.5

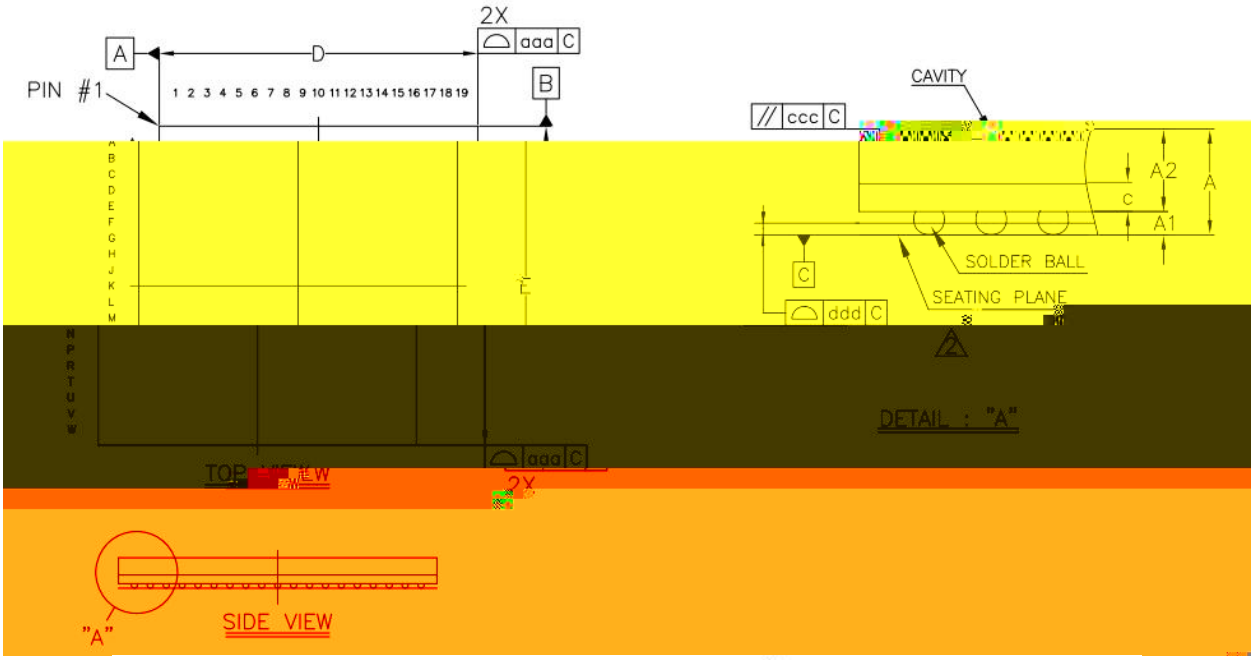
Advanced pass-through-compatible management packet transmit/receive support	Y
Managed ports on SMBus interface to external BMC	4
Auto-ARP reply over SMBus	Y
NC-SI Interface to an External BMC	Y
Standard DMTF NC-SI protocol support	Y
DMTF MCTP protocol over SMBus	Y
NC-SI HW arbitration	N
OS to BMC traffic	Y
L2 address filters	4
VLAN L2 filters	8
EtherType filters	4
Flex L4 port filters	16
Flex TCO filters	4
L3 address filters (IPv4)	4
L3 address filters (IPv6)	4
Build-in Temperature sensor	Y

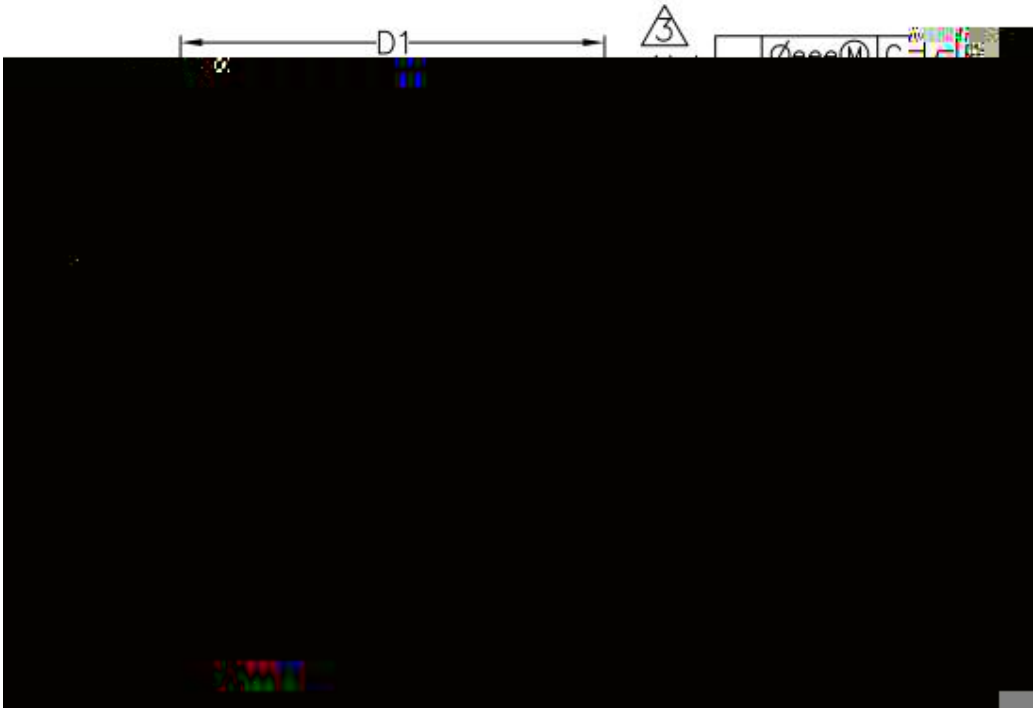
1.

Hardware implemented SM2/SM3/SM4 engine	Y
True Random number generato	

2

2.1


2X
aaa C
A
D
PIN #1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
B
CAVITY
ccc C
A2
A
c
A1
SOLDER BALL
C
SEATING PLANE
ddd C
DETAIL : "A"
TOP VIEW
aaa C
2X
"A"
SIDE VIEW


D1

A	1.17	1.24	1.31
A1	0.13	0.18	0.23
A2	1.01	1.06	1.11
c	0.32	0.36	0.40
b	0.20	0.25	0.30
D	12.90	13.00	13.10
E	12.90	13.00	13.10
D1	--	11.70	--
E1	--	11.70	--
e	--	0.65	--
aaa	0.10 BSC		
ccc	0.15 BSC		
ddd	0.13 BSC		
eee	0.15 BSC		
fff	0.08 BSC		
N	327		

Note:

1. Controlling dimension: millimeter
2. Primary datum C and seating plance are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum c.
4. The pattern of pin 1 fiducial is for reference only.
5. Refernce document: JEDEC publication 95 design guide 4.5

2.2

2.3

2.3.1

3.3V LVCMOS IO

scan_enable	G2	IN	Down	DFT
test_sel	F5	IN	Do	
test_mode_0	F1	IN	Do	
test_mode_1	F4	IN	Dow	
test_mode_2	F2	IN	Dow	
jtag_sel_0	E16	IN	Down	
jtag_sel_1	C19	IN	Down	
clk_tst_sel_0	E4	IN	Down	
clk_tst_sel_1	E1	IN	Down	
clk_tst_sel_2	E5	IN	Down	
clk_tst_sel_3	E2	IN	Down	
flash_sector	G4	IN	Down	0-64KB 1-256KB
flash_bypass	H1	IN	Down	flash
mng_det	F3	IN	Up	
sec_disable	G1	IN	Down	N/C
use_ext_phy	E3	IN	Down	RGMII PHY 4
xtal_in	R2	IN		25MHz
xtal_out	P2	OUT		
sec_mode	H2	IN		N/C
pe_rst_seq	B16	IN		
pe_aux_pwr_det	D15	IN	Down	WoL

2.3.2

n0_gphy_rset	U6	A	#0	2.49KΩ±1%
n0_led_0	K1	OUT	LED_0, Programmable LED which indicates by default activity, active high. Blink time 20-60ms adjustable, active high/low adjustable.	
n0_led_1	H4	OUT	LED_1, Programmable LED which indicates by default a 100Mbps Link, active high.	
n0_led_2	J2	OUT	LED_2, Programmable LED which indicates by default a 1000Mbps Link, active high.	
n0_mdi_p_0 n0_mdi_n_0	V6 W6	A A	In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transimit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.	
n0_mdi_p_1 n0_mdi_n_1	V5 W5	A A	In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transimit pair in 10Base-T and 100Base-TX.	
n0_mdi_p_2 n0_mdi_n_2	V4 W4	A A	In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.	
n0_mdi_p_3				

n0_rgmii_tx_2	M17	OUT		
n0_rgmii_tx_3	M16	OUT		
n0_rgmii_rx_0	N17	IN/OUT		#0 RGMII
n0_rgmii_rx_1	M15	IN/OUT		
n0_rgmii_rx_2	P16	IN/OUT		
n0_rgmii_rx_3	P17	IN/OUT		
n0_rgmii_txc	N16	OUT		#0 RGMII
n0_rgmii_tx_ctl	R16	OUT		
n0_rgmii_rxc	N15	IN	Down	#0 RGMII
n0_rgmii_rx_ctl	R17	IN	Down	
n0_rgmii_mdc	P15	OUT		#0 RGMII MDIO MDIO
n0_rgmii_mdio	T17	IN/OUT		1.5-10Kohm

2.3.4 #1

n0_dis_n	C17	IN	Up	#0
n1_dis_n	E17	IN	Up	#1
n2_dis_n	C18	IN	Up	#2
n3_dis_n	F16	IN	Up	#3
n1_gphy_rset	U9	A		#1 2.49KΩ±1%
n1_led_0	H3	OUT		LED_0, Programmable LED which indicates by default activity, active high. Blink time 20-60ms adjustable, active high/low adjustable.
n1_led_1	K2	OUT		LED_1, Programmable LED which indicates by default a 100Mbps Link, active high.
n1_led_2	H5	OUT		LED_2, Programmable LED which indicates by default a 1000Mbps Link, active high.
n1_mdi_p_0	V10	A		In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transimit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T
n1_mdi_n_0	W10	A		

				and 100Base-TX.
n1_mdi_p_1	V9	A		In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transimit pair in 10Base-T and 100Base-TX.
n1_mdi_n_1	W9	A		
n1_mdi_p_2	V8	A		In MDI mode, this is the third pair in 1000Base-T, i.e.,the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
n1_mdi_n_2	W8	A		
n1_mdi_p_3	V7	A		In MDI mode, this is the Fourth pair in 1000Base-T, i.e.,the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.
n1_mdi_n_3	W7	A		

2.3.5 #1

n1_rgmii_tx_0	M19	OUT		#1 RGMII
n1_rgmii_tx_1	P19	OUT		
n1_rgmii_tx_2	N19	OUT		
n1_rgmii_tx_3	U19	OUT		
n1_rgmii_rx_0	P18	IN/OUT		#1 RGMII
n1_rgmii_rx_1	V19	IN/OUT		
n1_rgmii_rx_2	R18	IN/OUT		
n1_rgmii_rx_3	N18	IN/OUT		
n1_rgmii_txc	U18	OUT		#1 RGMII
n1_rgmii_tx_ctl	T18	OUT		
n1_rgmii_rxc	L18	IN	Down	#1 RGMII
n1_rgmii_rx_ctl	T19	IN	Down	
n1_rgmii_mdc	R19	OUT		#1 RGMII MDIO MDIO 1.5-10Kohm
n1_rgmii_mdio	M18	IN/OUT		

n2_rgmii_tx_3	G18	OUT		
n2_rgmii_rx_0	H18	IN		#2 RGMII
n2_rgmii_rx_1	E19	IN		
n2_rgmii_rx_2	F19	IN		
n2_rgmii_rx_3	G19	IN		
n2_rgmii_txc	H19	OUT		#2 RGMII
n2_rgmii_tx_ctl	J18	OUT		
n2_rgmii_rxc	J19	IN	Down	#2 RGMII
n2_rgmii_rx_ctl	K18	IN	Down	
n2_rgmii_mdc	K19	OUT		#2 RGMII MDIO MDIO 1.5-10Kohm
n2_rgmii_mdio	L19	IN/OUT		

2.3.

				10Base-T and 100Base-TX.
n3_mdi_p_2	V16	A		In MDI mode, this is the third pair in 1000Base-T, i.e.,the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
n3_mdi_n_2	W16	A		
n3_mdi_p_3	V15	A		In MDI mode, this is the Fourth pair in 1000Base-T, i.e.,the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.
n3_mdi_n_3	W15	A		

2.3. #3 (4-)

n3_rgmii_tx_0	G16	OUT		#3 RGMII
n3_rgmii_tx_1	F17	OUT		
n3_rgmii_tx_2	G15	OUT		
n3_rgmii_tx_3	G17	OUT		
n3_rgmii_rx_0	H16	IN/OUT		#3 RGMII
n3_rgmii_rx_1	J15	IN/OUT		
n3_rgmii_rx_2	H15	IN/OUT		
n3_rgmii_rx_3	K15	IN/OUT		
n3_rgmii_txc	J16	OUT		#3 RGMII
n3_rgmii_tx_ctl	K16	OUT		
n3_rgmii_rxc	L15	IN	Down	#3 RGMII
n3_rgmii_rx_ctl	H17	IN	Down	
n3_rgmii_mdc	J17	OUT		#3 RGMII MDIO MDIO 1.5-10Kohm
n3_rgmii_mdio	K17	IN/OUT		

2.3.10

n0_gpio_0	D12	IN/OUT	#0 GPIO 0 Y G Y b

n1_gpio_0	E13	IN/OUT		#1 GPIO 0
n1_gpio_1	B15	IN/OUT		#1 GPIO 1
n2_gpio_0	D13	IN/OUT		#2 GPIO 0
n2_gpio_1	A17	IN/OUT		#2 GPIO 1
n3_gpio_0	E14	IN/OUT		#3 GPIO 0
n3_gpio_1	A18	IN/OUT		#3 GPIO 1
mng_gpio_0	D14	IN/OUT		CPU GPIO 0
mng_gpio_1	C14	IN/OUT		CPU GPIO 1

2.3.11

MII PHY NCSI BMC

mac SMBUS mode NC-SI mode

			D	
uart_srx	A14	IN	Down	CPU UART CPU
uart_stx	D11	OUT		
mng_ic_clk	K4	IN/OD	Up	CPU I2C pe_aux_pwr_det
mng_ic_data	P1	IN/OD	Up	CPU I2C pe_aux_pwr_det
mng_ic_smbsus_n		IN\		

rmii_tx_en/ ncsi_csr_dv	L4	OUT		Carrier Sense/Receive Data Valid
rmii_txd_0/ ncsi_rxd_0	T1	OUT		Received data signals from WX1860 to BMC
rmii_txd_1/ ncsi_rxd_1	L3	OUT		
mii_mdc	D3	OUT		MII MDIO
mii_md	C2	IN /OUT		

2.3.12 15

n0_ts1588_sdp_0	T2	IN/OUT		#0 TS1588 GPIO
n0_ts1588_sdp_1	L5	IN/OUT		
n0_ts1588_sdp_2	V1	IN/OUT		
n0_ts1588_sdp_3	M3	IN/OUT		
n1_ts1588_sdp_0	V2	IN/OUT		#1 TS1588 GPIO
n1_ts1588_sdp_1	M4	IN/OUT		
n1_ts1588_sdp_2	U2	IN/OUT		
n1_ts1588_sdp_3	P3	IN/OUT		
n2_ts1588_sdp_0	U3	IN/OUT		#2 TS1588 GPIO
n2_ts1588_sdp_1	N4	IN/OUT		
n2_ts1588_sdp_2	W2	IN/OUT		
n2_ts1588_sdp_3	M5	IN/OUT		
n3_ts1588_sdp_0	R3	IN/OUT		#3 TS1588 GPIO
n3_ts1588_sdp_1	R4	IN/OUT		
n3_ts1588_sdp_2	T3	IN/OUT		
n3_ts1588_sdp_3	N5	IN/OUT		

2.3.13

pe_wake_n	E15	OD	Up	PCIe WAKE# WOL
pxpor_res	J1	IN	Down	POR_BYPASS= 0: PXPOR_RES POR_BYPASS= 1: PXPOR_RES
por_bypass	G5	IN	Down	pxpor_res pxpor_res
perst_n	G3	IN		PCIe PERST#
pe_phy_resref	C10	A		PCIe PHY 200Ω (1% ,±100 ppm/ C)
pe_ref_clk_p	C8	A-in		PCIe 100MHz PCIe slot
pe_ref_clk_n	D8	A-in		
pe_tx_p_0	B13	A-out		PCIe PHY Gen2x4
pe_tx_n_0	A13	A-out		
pe_tx_p_1	B8	A-out		
pe_tx_n_1	A8	A-out		
pe_tx_p_2	B7	A-out		
pe_tx_n_2	A7	A-out		
pe_tx_p_3	B2	A-out		
pe_tx_n_3	A2	A-out		
pe_rx_p_0	B11	A-in		
pe_rx_n_0	A11	A-in		
pe_rx_p_1	B10	A-in		
pe_rx_n_1	A10	A-in		
pe_rx_p_2	B5	A-in		
pe_rx_n_2	A5	A-in		
pe_rx_p_3	B4	A-in		
pe_rx_n_3	A4	A-in		

2.3.14

spi_clk_div_0	A15	IN	Down	WOL 011 WOL 000 SPI clock 62.5MHz 000: ”divide by 2”, 31.25MHz 001: “divide by 4” 15.625MHz 010: “divide by 6”10.417MHz 011: “divide by 8”7.8125MHz 100: “divide by 10”6.25MHz 101: “divide by 16”3.90625MHz 110-111 not used.
spi_clk_div_1	E12	IN	Down	
spi_clk_div_2	B14	IN	Down	
spi_clk	B17	OUT		SPI flash
spi_cs_n	D16	OUT		
spi_si	C15	IN	Down	
spi_so	D17	OUT		

2.3.15

jrst_n	B18	IN	Down	JTAG
jtck	F15	IN	Down	
jtdi	B19	IN	Up	
jtdo	D18	OUT		
jtms	C16	IN/OUT	Up	

2.3.1

VCC33_N0_EFUSE	C5	EFUSE 3.3V
VCC33_N1_EFUSE	C4	
VCC33_N2_EFUSE	D5	
VCC33_N3_EFUSE	C3	

2.4

A1	GND_PEPHY_GD	
A2	PE_TX_N_3	PCIe 5Gbps SerDes
A3	GND_PEPHY_GD	
A4	PE_RX_N_3	PCIe 5Gbps SerDes
A5	PE_RX_N_2	PCIe 5Gbps SerDes
A6	GND_PEPHY_GD	
A7	PE_TX_N_2	PCIe 5Gbps SerDes
A8	PE_TX_N_1	PCIe 5Gbps SerDes
A9	GND_PEPHY_GD	
A10	PE_RX_N_1	PCIe 5Gbps SerDes
A11	PE_RX_N_0	PCIe 5Gbps SerDes
A12	GND_PEPHY_GD	
A13	PE_TX_N_0	PCIe 5Gbps SerDes
A14	UART_SRX	UART
A15	SPI_CLK_DIV_0	SPI clock divider bit[0]
A16	N0_GPIO_1	Lan0 GPIO bit[1]
A17	N2_GPIO_1	Lan2 GPIO bit[1]
A18	N3_GPIO_1	Lan3 GPIO bit[1]
A19	GND	
B1	GND_PEPHY_GD	
B2	PE_TX_P_3	PCIe 5Gbps SerDes
B3	GND_PEPHY_GD	
B4	PE_RX_P_3	PCIe 5Gbps SerDes
B5	PE_RX_P_2	PCIe 5Gbps SerDes
B6	GND_PEPHY_GD	
B7	PE_TX_P_2	PCIe 5Gbps SerDes
B8	PE_TX_P_1	PCIe 5Gbps SerDes
B9	GND_PEPHY_GD	
B10	PE_RX_P_1	PCIe 5Gbps SerDes
B11	PE_RX_P_0	PCIe 5Gbps SerDes
B12	GND_PEPHY_GD	

B13	PE_TX_P_0	PCIe 5Gbps SerDes
B14	SPI_CLK_DIV_2	SPI clock divider bit[2]
B15	N1_GPIO_1	Lan1 GPIO bit[1]
B16	PE_RST_SEQ	PCIe reset sequence control.
B17	SPI_CLK	SPI flash clock, max clock frequency is 50MHz
B18	JRST_N	JTAG reset
B19	JTDI	JTAG TDI
C1	MNG_BSY	Management busy indication
C2	MII_MD	NCSI PHY MDIO
C3	VCC33_N3_EFUSE	
C4	VCC33_N1_EFUSE	
C5	VCC33_N0_EFUSE	
C6	GND_TS_GND33A	
C7	VCC33A_TDC	
C8	PE_REF_CLK_P	PCIe 100MHz reference clock
C9	GND_PEPHY_GD	
C10	PE_PHY_RESREF	PCIe reference resistor
C11	GND_PEPHY_GD	
C12	PRB_HIT	Probe hit
C13	PRB_CLKOUT	Probe clock out
C14	MNG_GPIO_1	Managment GPIO bit [1]
C15	SPI_SI	SPI flash SI
C16	JTMS	JTAG JMS
C17	N0_DIS_N	Active low Lan0 disable
C18	N2_DIS_N	Active low Lan2 disable
C19	JTAG_SEL_1	JTAG select bit[1]
D1	PRB_EN	Probe enable, 0 for normal function
D2	PCIE_BSY	PCIe link busy indication
D3	MII_MDC	NCSI PHY MDIO
D4	VCC33_EFUSE	
D5	VCC33_N2_EFUSE	
D6	GND_PEPHY_GD	
D7	VCC11A_PE_VP	
D8	PE_REF_CLK_N	PCIe PHY reference clock
D9	VCC11A_PE_VP	
D10	GND_PEPHY_GD	
D11	UART_STX	UART

D12	N0_GPIO_0	
D13	N2_GPIO_0	
D14	MNG_GPIO_0	
D15	PE_AUX_PWR_DET	PCIe Aux power available
D16	SPI_CS_N	SPI flash CS_N
D17	SPI_SO	SPI flash SO
D18	JTDO	JTAG JTDO
D19	N2_RGMII_TX_0	RGMII interface
E1	CLK_TST_SEL_1	Test clock selection, only
E2	CLK_TST_SEL_3	Test clock selection, only
E3	USE_EXT_PHY	External PHY selection, 1'b0 to use internal 1000Base-T PHY, 1'b1 to use external RGMII PHY. It controls all 4 ports.
E4	CLK_TST_SEL_0	Test clock selection, only
E5	CLK_TST_SEL_2	Test clock selection, only
E6	VCC11A_PE_VPTX3	
E7	VCC11A_PE_VPTX2	
E8	VCC33A_PE_VPH	
E9	VCC11A_PE_VPTX1	
E10	VCC11A_PE_VPTX0	
E11	VCCK_VMAIN	
E12	SPI_CLK_DIV_1	SPI clock divider control bit[1]
E13	N1_GPIO_0	Lan1 GPIO bit[0]
E14	N3_GPIO_0	Lan3 GPIO bit[0]
E15	PE_WAKE_N	Active low WAKE# on PCIe slot.
E16	JTAG_SEL_0	JTAG selection bit[0]
E17	N1_DIS_N	Active low Lan1 disable
E18	N2_RGMII_TX_1	RGMII interface
E19	N2_RGMII_RX_1	RGMII interface
F1	TEST_MODE_0	Test mode, 0 for normal function
F2	TEST_MODE_2	Test mode, 0 for normal function
F3	MNG_DET	Management available, 1 for normal function
F4	TEST_MODE_1	Test mode, 0 for normal function
F5	TEST_SEL	Test selection, 0 for normal function
F15	JTCK	JTAG TCK
F16	N3_DIS_N	Active low Lan3 disable
F17	N3_RGMII_TX_1	RGMII interface
F18	N2_RGMII_TX_2	RGMII interface

F19	N2_RGMII_RX_2	RGMII interface
G1	SEC_DISABLE	1'b1 to disable IPsec and LinkSec
G2	SCAN_ENABLE	For DFT, 0 for normal function
G3	PERST_N	PERST# at PCIe slot
G4	FLASH_SECTOR	0 for 64KB, 1 for 256KB
G5	POR_BYPASS	1 to by pass chip internal POR module and use PXPOR_RES as active low power on reset
G7	VCC3IO	
G8	GND	
G9	GND	
G10	VCCK	
G11	VCC3IO	
G12	VCC3IO	
G13	GND	
G15	N3_RGMII_TX_2	RGMII interface
G16	N3_RGMII_TX_0	RGMII interface
G17	N3_RGMII_TX_3	RGMII interface
G18	N2_RGMII_TX_3	RGMII interface
G19	N2_RGMII_RX_3	RGMII interface
H1	FLASH_BYPASS	0 for normal function
H2	SEC_MODE	1 to enable sec mode
H3	N1_LED_0	Lan LED
H4	N0_LED_1	Lan LED
H5	N1_LED_2	Lan LED
H7	VCCK	
H8	GND	
H9	GND	
H10	GND	
H11	GND	
H12	GND	
H13	VCCK	
H15	N3_RGMII_RX_2	RGMII interface
H16	N3_RGMII_RX_0	RGMII interface
H17	N3_RGMII_RX_CTL	RGMII interface
H18	N2_RGMII_RX_0	RGMII interface
H19	N2_RGMII_TXC	RGMII interface
J1	PXPOR_RES	Active High reset to reset chip intern POR. When POR_BYPASS=1, it is the active low power on reset.

J2	N0_LED_2	Lan LED
J3	N2_LED_1	Lan LED
J4	N3_LED_0	Lan LED
J5	N3_LED_2	Lan LED
J7	VCC3IO	
J8	GND	
J9	GND	
J10	GND	
J11	GND	
J12	GND	
J13	VCC18IO_25V	
J15	N3_RGMII_RX_1	RGMII interface
J16	N3_RGMII_TXC	RGMII interface
J17	N3_RGMII_MDC	RGMII MDIO for extern PHY control
J18	N2_RGMII_TX_CTL	RGMII interface
J19	N2_RGMII_RXC	RGMII interface
K1	N0_LED_0	Lan LED
K2	N1_LED_1	Lan LED
K3	MNG_IC_SMBSUS_N	SMbus for management
K4	MNG_IC_CLK	SMbus for management
K5	RMII_CSR_DV	NCSI interface
K7	VCCK	
K8	GND	
K9	GND	
K10	GND	
K11	GND	
K12	GND	
K13	VCCK	
K15	N3_RGMII_RX_3	RGMII interface
K16	N3_RGMII_TX_CTL	RGMII interface
K17	N3_RGMII_MDIO	RGMII MDIO for extern PHY control
K18	N2_RGMII_RX_CTL	RGMII interface
K19	N2_RGMII_MDC	RGMII MDIO for extern PHY control
L1	N2_LED_2	Lan LED
L2	N3_LED_1	Lan LED
L3	RMII_TXD_1	NCSI interface
L4	RMII_TX_EN	NCSI interface
L5	N0_TS1588_SDP_1	TS1588 GPIO

L7	VCC3IO	
L8	GND	
L9	GND	
L10	GND	
L11	GND	
L12	GND	
L13	VCC18IO_25V	
L15	N3_RGMII_RXC	RGMII interface
L16	N0_RGMII_TX_1	RGMII interface
L17	N0_RGMII_TX_0	RGMII interface
L18	N1_RGMII_RXC	RGMII interface
L19	N2_RGMII_MDIO	RGMII MDIO for extern PHY control
M1	N2_LED_0	Lan LED
M2	RMII_RXD_0	NCSI interface
M3	N0_TS1588_SDP_3	TS1588 GPIO
M4	N1_TS1588_SDP_1	TS1588 GPIO
M5	N2_TS1588_SDP_3	TS1588 GPIO
M7	VCCK	
M8	GND	
M9	GND	
M10	GND	
M11	GND	
M12	GND	
M13	VCCK	
M15	N0_RGMII_RX_1	RGMII interface
M16	N0_RGMII_TX_3	RGMII interface
M17	N0_RGMII_TX_2	RGMII interface
M18	N1_RGMII_MDIO	RGMII MDIO for extern PHY control
M19	N1_RGMII_TX_0	RGMII interface
N1	MNG_IC_SMBALT_N	SMbus for management
N2	VCC11A_PLL	
N3	GND11A_PLL	
N4	N2_TS1588_SDP_1	TS1588 GPIO
N5	N3_TS1588_SDP_3	TS1588 GPIO
N7	GND	
N8	VCC33A_GIGA	
N9	GND	
N10	VCC33A_GIGA	

N11	GND	
N12	VCC33A_GIGA	
N13	VCC33A_GIGA	
N15	N0_RGMII_RXC	RGMII interface
N16	N0_RGMII_TXC	RGMII interface
N17	N0_RGMII_RX_0	RGMII interface
N18	N1_RGMII_RX_3	RGMII interface
N19	N1_RGMII_TX_2	RGMII interface
P1	MNG_IC_DATA	SMbus for management
P2	OSC_IO	External oscillator
P3	N1_TS1588_SDP_3	TS1588 GPIO
P4	GND	
P5	GND	
P7	VCC11A_A10	
P8	GND	
P9	VCC11A_A10	
P10	GND	
P11	VCC11A_A10	
P12	GND	
P13	VCC11A_A10	
P15	N0_RGMII_MDC	RGMII MDIO for extern PHY control
P16	N0_RGMII_RX_2	RGMII interface
P17	N0_RGMII_RX_3	RGMII interface
P18	N1_RGMII_RX_0	RGMII interface
P19	N1_RGMII_TX_1	RGMII interface
R1	RMII_REF_CLK	NCSI interface
R2	OSC_I	External oscillator
R3	N3_TS1588_SDP_0	TS1588 GPIO
R4	N3_TS1588_SDP_1	TS1588 GPIO
R5	GND	
R15	GND	
R16	N0_RGMII_TX_CTL	RGMII interface
R17	N0_RGMII_RX_CTL	RGMII interface
R18	N1_RGMII_RX_2	RGMII interface
R19	N1_RGMII_MDC	RGMII MDIO for extern PHY control
T1	RMII_TXD_0	NCSI interface
T2	N0_TS1588_SDP_0	TS1588 GPIO
T3	N3_TS1588_SDP_2	TS1588 GPIO

T4	GND	
T5	VCC11A_CEN	
T6	GND	
T7	VCCK	
T8	GND	
T9	VCCK	
T10	GND	
T11	VCCK	
T12	GND	
T13	VCCK	
T14	GND	
T15	VCC33A_CEN	
T16	GND	
T17	N0_RGMII_MDIO	RGMII MDIO for extern PHY control
T18	N1_RGMII_TX_CTL	RGMII interface
T19	N1_RGMII_RX_CTL	RGMII interface
U1	RMII_RXD_1	NCSI interface
U2	N1_TS1588_SDP_2	TS1588 GPIO
U3	N2_TS1588_SDP_0	TS1588 GPIO
U4	GND	
U5	G0_RTT	
U6	N0_GPHY_RSET	
U7	G0_OPIN_PAD	
U8	G1_RTT	
U9	N1_GPHY_RSET	
U10	G1_OPIN_PAD	
U11	G2_RTT	
U12	N2_GPHY_RSET	
U13	G2_OPIN_PAD	
U14	G3_RTT	
U15	N3_GPHY_RSET	
U16	G3_OPIN_PAD	
U17	GND	
U18	N1_RGMII_TXC	RGMII interface
U19	N1_RGMII_TX_3	RGMII interface
V1	N0_TS1588_SDP_2	TS1588 GPIO
V2	N1_TS1588_SDP_0	TS1588 GPIO
V3	N0_MDI_P_3	1000Base-T serdes

V4	N0_MDI_P_2	1000Base-T serdes
V5	N0_MDI_P_1	1000Base-T serdes
V6	N0_MDI_P_0	1000Base-T serdes
V7	N1_MDI_P_3	1000Base-T serdes
V8	N1_MDI_P_2	1000Base-T serdes
V9	N1_MDI_P_1	1000Base-T serdes
V10	N1_MDI_P_0	1000Base-T serdes
V11	N2_MDI_P_3	1000Base-T serdes
V12	N2_MDI_P_2	1000Base-T serdes
V13	N2_MDI_P_1	1000Base-T serdes
V14	N2_MDI_P_0	1000Base-T serdes
V15	N3_MDI_P_3	1000Base-T serdes
V16	N3_MDI_P_2	1000Base-T serdes
V17	N3_MDI_P_1	1000Base-T serdes
V18	N3_MDI_P_0	1000Base-T serdes
V19	N1_RGMII_RX_1	RGMII interface
W1	GND	
W2	N2_TS1588_SDP_2	TS1588 GPIO
W3	N0_MDI_N_3	1000Base-T serdes
W4	N0_MDI_N_2	1000Base-T serdes
W5	N0_MDI_N_1	1000Base-T serdes
W6	N0_MDI_N_0	1000Base-T serdes
W7	N1_MDI_N_3	1000Base-T serdes
W8	N1_MDI_N_2	1000Base-T serdes
W9	N1_MDI_N_1	1000Base-T serdes
W10	N1_MDI_N_0	1000Base-T serdes
W11	N2_MDI_N_3	1000Base-T serdes
W12	N2_MDI_N_2	1000Base-T serdes
W13	N2_MDI_N_1	1000Base-T serdes
W14	N2_MDI_N_0	1000Base-T serdes
W15	N3_MDI_N_3	1000Base-T serdes
W16	N3_MDI_N_2	1000Base-T serdes
W17	N3_MDI_N_1	1000Base-T serdes
W18	N3_MDI_N_0	1000Base-T serdes
W19	GND	

3

3.1

	-65		140	° C
Tj(PN)	-55		125	° C
VCCK VCC11A	-0.1	1.1	1.155	V
VCC11A_PE,VCC11A_A10,VCC11A_CEN,VCC11A_PLL	-0.1	1.1	1.155	V
VCC3IO,VCC33A VCC33	-0.4	3.3	3.7	V
VCC18IO_25V	-0.4	3.3	3.7	V

3.2

	-40		85	° C
VCCK VCC11A	1.045	1.1	1.155	V
VCC11A_PE,VCC11A_A10,VCC11A_CEN,VCC11A_PLL	1.045	1.1	1.155	V
VCC3IO,VCC33A VCC33	3.135	3.3	3.465	V
VCC18IO_25V	3.135	3.3	3.465	V

3.3

IO reference voltage	Vref		3.0	3.3	3.6	V
Input low voltage	Vil				0.8	V
Input high voltage	Vih		2.0			V
Input low current	Iil	Vin=0V	-20		0	μA
Input high current	Iih	Vin=Vref-Vref,max	0		200	μA
Output low voltage	Vol	Iol=4mA,Vref=min	0		400	mV
Output high voltage	Voh	IOh=-4mA,Vref=min	2.4		Vref	V

3.4

The WX1860 is designed to support the standard DMTF NCSI interface. For NCSI I/F timing specification see the following table.

Tckf	NCSI_REF_CLK Frequency		50		MHz
Rdc	NCSI_REF_CLK duty cycle	35		65	%
Racc	NCSI_REF_CLK accuracy			100	ppm
Tco	Clock-to-out (10 pF =< cload <=50 pF) NCSI_RXD[1:0], NCSI_CSR_DV Data valid from NCSI_REF_CLK rising edge	2.5		12.5	ns
Tsu	NCSI_TXD[1:0], NCSI_TX_EN Data Setup to NCSI_CLK_IN rising edge	3			ns
Thold	NCSI_TXD[1:0], NCSI_TX_EN Data hold from NCSI_REF_CLK rising edge	1			ns
Tor	NCSI_RXD[1:0], NCSI_CSR_DV Output Time rise	0.5		6	ns
Tof	NCSI_RXD[1:0], NCSI_CSR_DV Output Time fall	0.5		6	ns
Tckr/Tckf	NCSI_REF_CLK Rise/Fall Time	0.5		3.5	ns

3.5

The 25 MHz reference clock of the WX1860 can be supplied either from a crystal or from an external oscillator. The recommended solution is to use a crystal.

Frequency	-	-	25	-	MHz

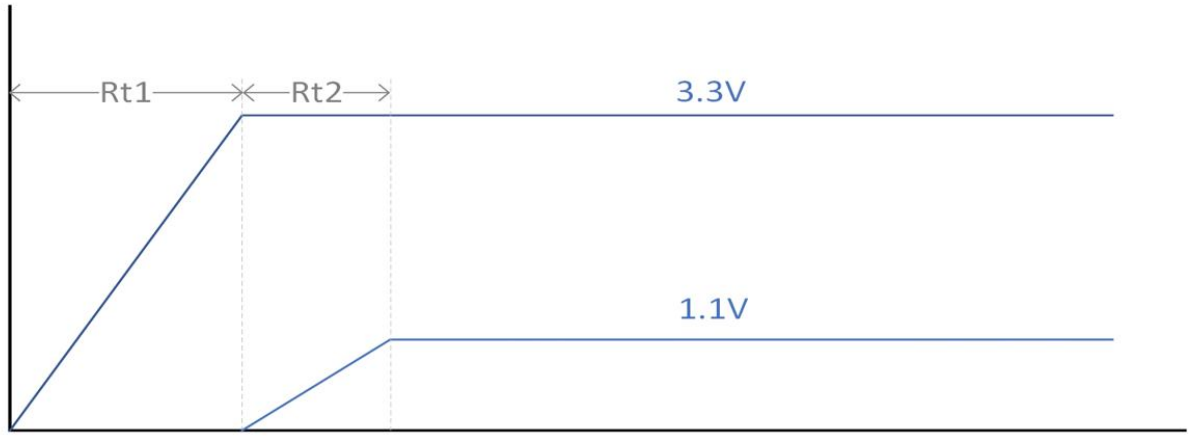
Vibration mode			Fundamental		
Frequency Stability	Ta=0-70	-30		+30	ppm
Frequency Tolerance	Ta=25	-50		+50	ppm
Load Capacitance			20		pf

Frequency	-	-	25	-	MHz
Frequency Stability	Ta=0-70	-30		+30	ppm
Frequency Tolerance	Ta=25	-50		+50	ppm
Duty Cycle		40		60	%
Broadband Peak-to-peak Jitter				200	ps
Vpeak-to-peak		3.135	3.3	3.465	V
Rise time 10%-90%				10	ns
Fall time 10%-90%				10	ns
Operation temperature Range		0		70	

3.5

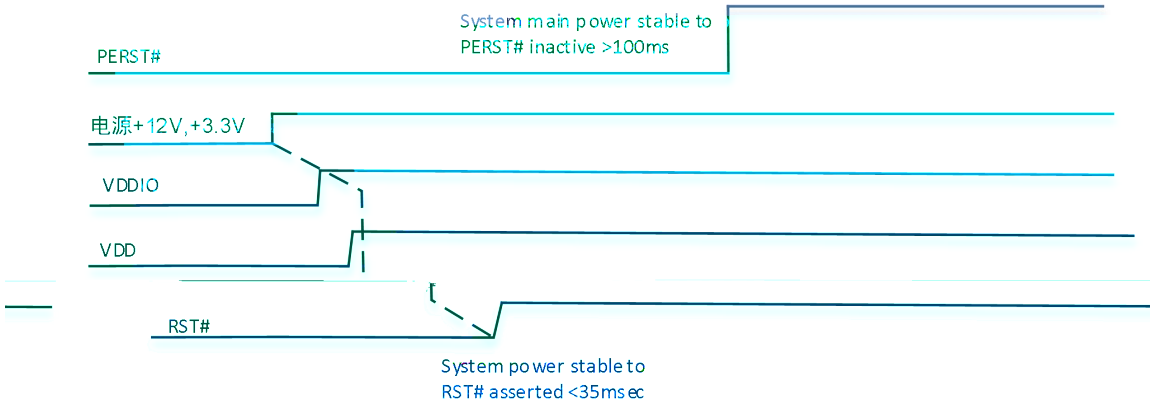
GPHY IP 1.1V 3.3V 5ms 3.3V rise time 1ms

3.3V 1.1V



Rt1	3.3V rise time	1	-	100	ms
Rt2	3.3V ready to 1.1V ready time	-5	-	-	ms

WX1860 RST# J1 PERST# G3



VDDIO VCCIO VCC33A VDD VCCK VCC11A

3.6

WX1860 socket socket Z390-A PCI
4 CH1 CH2 CH3 CH4
1000M WX1860A4/WX1860AL4 70

4

winbond	W25Q80DV
microchip	SST25VF080B
	GD25Q80

5

1	WX1860A2		0 -70 ,40nm,2	2
2	WX1860A4		0 -70 ,40nm,4	4
3	WX1860AL1		-40 -85 ,40nm,1 SM2/SM3/SM4	1
4	WX1860AL2		-40 -85 ,40nm,2 SM2/SM3/SM4	2
5	WX1860AL4		-40 -85 ,40nm,4 SM2/SM3/SM4	4

1 N0 2 N0 N1 N2 N3
N0 N1 N2 N3